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## **iDev Modem Development Platform**

### **Board Specifications - Preliminary**

Ver 1.4

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## **Revisions:**

<b>Ver.</b>	<b>Date</b>	<b>Author</b>	<b>Description</b>
1.0	3/2007	Yuval Y.	Initial version
1.1	4/2007	Yuval Y.	
1.2	7/2007	Yuval Y.	FPGAs changed from Xilinx to Altera Added support for DSP module .
1.3	9/2007	Yuval Y.	Integrating module into single board. Changing to Stratix-II-130-GX.

## **1 Introduction**

The iDev is an AdvancedTCA form-factor board designed to support the development of advanced modem (i.e XDSL, WiMax , DVB-H , WLAN). The board includes the resources required for the modem implementations and debugging accessories. This document describes the board including details of the digital and debug sections of the modem. The AFE is covered by a separate document and is not supported under the standard configuration.

The Modem can be operated in an ATCA chassis or in stand alone mode.

Although as previously stated, the modem can be operated inside an ATCA chassis - it is not compliant to the PICMG 3.x standard. The main deviation from this standard is that ATCA management interface is not supported. Also only a single switch at slot on is supported (no redundancy).

## **2 Block Diagram**

The iDev Modem block diagram is illustrated in Figure 1.

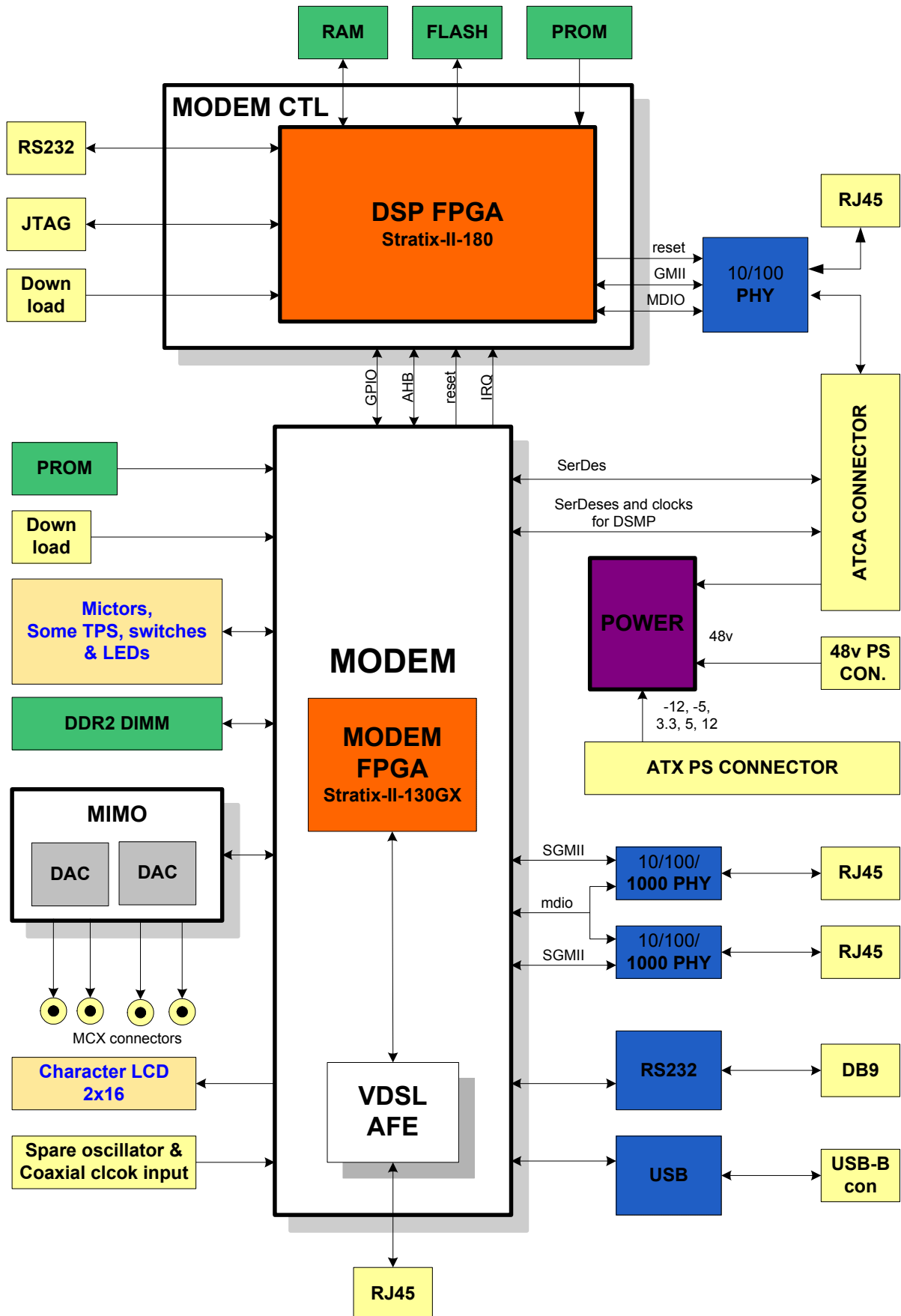


Figure 1: iDev Modem block diagram

## 3 iDev Platform Description

### 3.1 Modem block

The MODEM FPGA is an Altera Stratix2-130-GX (EP2SGX130GF1508C5) and can be used for modem implementation.

The MODEM main interfaces are:

- 2 x Ethernet interface - (10/100/1000 Ethernet link).
- 2 x Serdes Ethernet interface (1Gbps).
- External Memory interfaces (ZBT SRAM, DDR2 DIMM socket).
- AHB interface – for DSP FPGA.
- Dual ADC/DAC for wireless MIMO support.
- VDSL3 AFE Interface – not supported under standard configuration.

In addition, several debug interfaces are made available:

- Mictor connectors for convenient logic analyzer interface.

The FPGA firmware is downloaded upon power up from an Altera serial flash prom and can be downloaded also with an Altera download cable (through a JTAG connector).

### 3.2 External Memory Resources

The DSM FPGA is connected to several external memory resources:

- ZBT SRAM – 4 Megabits of Zero Bus Turnaround SRAM organized as 256K x 18. It can be expanded to 16 megabits, and an x36 organization is also supported. The SRAM can be clocked up to 166 MHz.
- DDR2 DIMM socket – a DDR2 240 pin socket that may hold up to 2 gigabytes of non ECC DDR2 SDRAM. A DDR2 module data bus width is 64 bits.

### 3.3 DSP block

The DSP FPGA is an Altera Stratix2-180 (EP2S180F1508C5) and can be used for DSP CPU implementation (i.e CEVA-X DSP).

The DSP main interfaces are:

- 1 x Ethernet interface - (10/100/1000 Ethernet link).
- AHB interface – for MODEM FPGA.
- RS232 , JTAG